UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,098	03/29/2001	Thomas D. Fletcher	42390P9006	8394

7590 11/20/2002

Cynthia Thomas Faatz
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER
NGUYEN, MINH T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,098	FLETCHER ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,18-21 and 28-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9-11,28-30,37 and 38* is/are rejected.

7)☒ Claim(s) *4,8,18-21 and 31-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicants' amendment filed on 9/17/02 has been received and entered in the case. The amendment and argument presented therein overcome the informality objections and indefiniteness rejection, and therefore, are withdrawn. New ground of rejection necessitated by the amendment is set forth below. This action is FINAL.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Method and Apparatus for Correcting a Clock Duty Cycle in a Clock Distribution Network".

Claim Objections

3. Claims 6-7, 18, 31, 33 and 35-36 are objected to because of the following informalities:

In claim 6, line 8, "the distributed global clock signal" should be changed to -- a distributed global clock signal -- to avoid antecedent basis problem because the clock distribution circuitry receives the global clock signal and distributes the global clock signal as a distributed global clock signal, i.e., the distributed global clock signal is not the same as the global clock signal. In other word, the global clock signal is the input signal to the clock

distribution circuitry and the distributed clock signal is the output signal from the clock distribution circuitry.

In claim 7, line 4, the term "includes the duty cycle correction circuit" should be changed to -- connected to the duty cycle correction circuit -- to avoid misdescriptive problem because it does not make sense for a node to include a circuit.

In claim 18, lines 7-8, "a duty cycle of the first clock signal at the receiving points" should be changed to -- duty cycle of distributed first clock signals at the receiving points -- since each of the distributed first clock signals at each of the receiving points are different signals.

In claim 31, "the circuit" recited on line 4 should be changed to --the duty cycle correction circuit -- to avoid antecedent basis problem.

In claim 33, line 1, "33" should be changed to -- 32 --.

In claim 35, line 5, "an output" should be changed to -- a first output --.

In claim 36, line 6, "an output" should be changed to -- a second output -- to clearly distinguish this output from the output recited in claim 35.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 37-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 37, the term "the input clock signal" recited on line 4 lacks clear antecedent basis, i.e., it is unclear if this is referring to the distributed clock signal recited on line 2. The recitation that the duty cycle correction circuit is to receive the distributed clock signal and to generate a reference voltage signal appears to be misdescriptive because a duty cycle correction circuit is for correcting the duty cycle of a clock signal by generating a corrected clock signal, it does not make any sense for a duty cycle correction circuit to generate a reference voltage signal as recited.

As per claim 38, this claim is rejected because of the indefiniteness of claim 37.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-7, 9-11, 28-30 and 37-38 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,398,262, issued to Ahuja (a copy of the Ahuja reference is included in the previous Office Action).

As per claim 1, Ahuja discloses an apparatus (Fig. 2) comprising:

a clock distribution network 20 (the entire circuitry that receives the INCLK clock signal and distributes this clock signal through out the microprocessor circuit 10) to distribute a clock signal INCLK on an integrated circuit chip (the microprocessor circuit 10 is an integrated circuit chip, column 4, lines 30-33); and

a duty cycle correction circuit (the combination of circuits 14, 17, 16, 12 and 13, this combination is seen as a duty cycle correction circuit having an input terminal which receives the clock signal CMINCLK and an output terminal which outputs the clock signal GCLK because the duty cycle of the clock signal INCLK which is input to the duty cycle correction circuit as signal CMINCLK is adjusted at the output terminal, i.e., the clock signal GCLK is the corrected duty cycle of the clock signal INCLK) at a receiver (the input terminal of the block circuit 12 which receives the distributed clock signal CMINCLK) in the clock distribution network 20 (the input node of the block circuit 12 is clearly inside the clock distribution network 20), the duty cycle correction circuit to correct the duty cycle of a distributed clock signal CMINCLK received at the receiver.

As per claim 2, Ahuja further discloses the duty cycle correction circuit includes

a feedback path between an input and an output of the duty cycle correction circuit (the path through the circuits 14, 17 and 16), the feedback path to control a delay of a circuit path in the duty cycle correction circuit to correct the duty cycle (the feedback path carries the feedback signal FCLK, and the signal FCLK is compared and compensated by the PLL circuit 12).

As per claim 3, since the GCLK clock signal is the corrected clock signal INCLK having skew-free, the duty cycle of the GCLK clock signal is substantial 50% when the duty cycle of the input clock signal INCLK is about 50%.

As per claim 5, Ahuja further discloses a smart buffer circuit 21 (the area buffer 21) coupled to the duty cycle correction circuit, since the Ahuja's smart buffer circuit 21 is buffered between the duty cycle correction circuit and the load UNIT1, it is seen as to provide proper operation of the duty cycle correction circuit over a range of loads to be coupled to the duty cycle correction circuit.

As per claim 6, Ahuja discloses a clock distribution network (Fig. 2) comprising:

clock generation circuitry (the circuitry which generates the clock signal INCLK) at a first location (the location which houses the clock generation circuitry) to generate a global clock signal INCLK;

clock distribution circuitry (all the lines and circuitry in the clock distribution network 20 which distribute the global clock signal INCLK to different paths) to distribute the global clock signal INCLK on an integrated circuit chip (the microprocessor circuit chip 10, column 3, lines 30-35) from the clock generation circuitry to a receiving point (the terminal which receives the clock signal CMINCLK) at a second, different location on the integrated circuit chip (as shown, the terminal which carries the CMINCLK signal is on the integrated circuit chip 10, and this receiver point is on different location from the location which houses the clock generation circuitry); and

a duty cycle correction circuit (the circuits 14, 17, 16, 12 and 13, this combination is seen as a duty cycle correction circuit having an input terminal which receives the clock signal CMINCLK and an output terminal which outputs the clock signal GCLK because the duty cycle of the clock signal INCLK which is input to the duty cycle correction circuit as signal CMINCLK is adjusted at the output terminal, i.e., the clock signal GCLK is the corrected duty

cycle of the clock signal INCLK) at the receiving point (the input terminal of the duty cycle circuit is the receiving point) to correct the duty cycle of the distributed global clock signal CMINCLK received via the clock distribution circuitry.

As per claim 7, Ahuja further discloses the clock distribution circuitry distributes the global clock signal INCLK to a plurality of receiving points (the nodes on lines 31, 23, ,,,, 40n) and wherein each of the plurality of receiving points connects to the duty cycle correction circuit (because these nodes connected to the duty cycle correction circuit).

As per claim 9, Ahuja further discloses the duty cycle correction circuit includes

a feedback path between an input and an output of the duty cycle correction circuit (the line which connects the circuits 14, 17 and 16), the feedback path to control a delay of a circuit path in the duty cycle correction circuit to correct the duty cycle (the feedback path carries the feedback signal FCLK, and the signal FCLK is compared and compensated by the PLL circuit 12).

As per claim 10, the recited at least one variable delay element reads on the delay caused by the input buffer 11, i.e., the dummy input buffer 16 is added to compensate for the delay caused by the input buffer 11. The recited signal flows through the dummy delay buffer 16 is delayed by the delay caused by the dummy delay buffer 16.

As per claim 11, this claim is rejected for the same reason noted in claim 3.

As per claim 28, this claim is merely a method to operate an apparatus having elements and connections recited in claim 1, since Ahuja teaches the apparatus, he inherently teaches the method to operate the apparatus.

As per claims 29-30, these claims are rejected for the same reasons noted in claims 2-3, respectively.

As per claim 37, due to the indefiniteness problem noted in section 4 above, the recited function of the duty cycle correction circuit and the clock generation circuit are assumed to read on the PLL circuit 12 because the PLL circuit 12 includes a lowpass filter to generate a reference voltage signal and a VCO circuit which generates the clock signal based on the reference voltage signal.

As per claim 38, the multiple clock signals are on the lines 31, 32, ... 40n, in Fig. 2.

Response to Arguments

6. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

7. Claims 18-21 are allowed after amended to overcome the objection noted in section 3 above.

Claims 18-21 are allowed because the prior art of record fails to disclose or suggest an integrated circuit chip which includes a plurality of duty cycle correction circuits at receiving points in the clock distribution network wherein the clock generation circuit, the clock distribution network and the plurality of duty cycle correction circuits are in an integrated circuit chip.

8. Claims 4, 8 and 31-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 4 is allowable because the prior art of record fails to disclose or suggest an apparatus which includes a frequency multiplying circuit coupled to the duty cycle correction circuit for providing an output clock signal having a frequency which is a multiple of the distributed clock signal.

Claim 8 is allowable for the same reason noted in claim 4.

Claim 31-33 are allowable because the prior art of record fails to disclose or suggest an apparatus which includes a sense amplifier circuit having a threshold voltage which is equal to one half of the supply voltage in the feedback path of the duty cycle correction circuit as recited in claim 31.

Claims 34-36 are allowable because the prior art of record fails to disclose or suggest an apparatus which includes a smart buffer circuit for adjusting the drive strength of the output driver in the duty cycle correction circuit as recited in claim 34.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

MN
November 16, 2002